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Applicant : King Jien Chui
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3 **AMENDMENTS TO THE CLAIMS**

4 This listing of claims will replace all prior versions, and listing, of claims in the
5 application:

6

7 Listing of claims:

8

- 9 1. (CURRENTLY AMENDED) A method of forming a semiconductor device
10 comprising:
11 a) forming a gate structure over a substrate being doped with a first
12 conductivity type impurity;
13 b) performing a doped depletion region implantation by implanting ions being a
14 second conductive type into the substrate to form doped depletion
15 regions; and
16 c) performing a S/D implantation by implanting ions being the second
17 conductivity type into the substrate to form source and drain regions
18 adjacent to said gate structure; at least a portion of the doped depletion
19 regions are directly beneath and separated from said source and drain
20 regions;
21 (1) said doped depletion regions having an impurity concentration and
22 thickness so that said doped depletion regions are depleted due to a
23 built-in potential created between said doped depletion regions and
24 said substrate;
25 said doped depletion regions having an impurity concentration so
26 that a built-in junction potential between said doped depletion
27 regions and said substrate forms depletion regions in the substrate
28 between the source and drain regions and the doped depletion
29 regions;

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1 said depletion regions have a net impurity concentration of the
2 first conductivity type.

3

4 2. (CURRENTLY AMENDED) The method of claim 1 wherein said doped
5 depletion regions are not formed directly under said gate structure.

6

7 3. (CANCELED)

8

9 4.(CURRENTLY AMENDED) The method of claim 1 which further includes said
10 doped depletion regions having an impurity concentration so that a built-in
11 junction potential between said doped depletion regions and said substrate
12 forms depletion regions in the substrate between the source and drain
13 regions and the doped depletion ~~region~~ regions; said depletion regions
14 have a net impurity concentration of the first conductivity type;
15 said depletion regions have a net impurity concentration between
16 1E16 to 5E18 atom/cc.

17

18 5. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
19 implanting ions of the first impurity type into said substrate between said
20 source and drain regions and said doped depletion regions.

21

22 6. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
23 performing an implant type selected from the group consisting of Halo
24 implant, threshold voltage implant, and a field implant, that implant ions of
25 the first impurity type into said substrate at least between said source and
26 drain regions and said doped depletion regions.

27

28 7. (CURRENTLY AMENDED) The method of claim 1 wherein a region of said
29 substrate between said source[/] and drain regions and said doped

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- 1 depletion regions has a concentration of the first conductivity type impurity
2 between 1E16 to 1E18 atom/cc; a channel region in said substrate under
3 said gate structure; said channel region has a concentration of a second
4 type impurity between 1E16 to 1E18 atom/cc.
- 5
- 6 8. (PREVIOUSLY PRESENTED) The method of claim 1 wherein said doped
7 depletion regions are fully depleted.
- 8
- 9 9. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
10 performing LDD implantation by implanting ions being the second
11 conductivity type into the substrate using the gate structure as a mask to
12 form LDD regions.
- 13
- 14 10. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
15 performing a LDD implantation by implanting ions being the second
16 conductivity type into the substrate using the gate structure as a mask to
17 form LDD regions;
18 the LDD regions are formed before the doped depletion regions.
- 19
- 20 11. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
21 performing a LDD implantation by implanting ions being the second
22 conductivity type into the substrate using the gate structure as a mask to
23 form LDD regions;
24 wherein the doped depletion regions are formed after the LDD regions.
- 25
- 26 12. (PREVIOUSLY PRESENTED) The method of claim 1 wherein said first
27 conductivity type is p-type and said substrate has a boron concentration
28 between 1E17 to 1E19 atom/cc.
- 29

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- 1 13. (PREVIOUSLY PRESENTED) The method of claim 1 wherein said first
2 conductivity type is n-type and said substrate has an As or P concentration
3 between 1E 17 to 1E 19 atom/cc.
4
5 14. (PREVIOUSLY PRESENTED) The method of claim 1 wherein said substrate
6 is comprised of Si or SiGe or strained Si, or relaxed SiGe or strained Ge.
7
8 15. (ORIGINAL) The method of claim 1 wherein said gate structure has a channel
9 width between 0.04 and 0.5 μm .
10
11 16. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
12 performing a LDD implantation by implanting ions being the second
13 conductivity type into the substrate using the gate structure as a mask to
14 form LDD regions; the LDD implantation is performed by implanting As ions
15 at a dose between 5E14 and 1E16 atoms /cm², at an energy between 1keV
16 and 10 keV.
17 17. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
18 performing a LDD implantation by implanting ions being the second
19 conductivity type into the substrate using the gate structure as a mask to
20 form LDD regions;
21 the LDD implantation is performed by implanting Boron ions at a dose between
22 1E14 and 5E15 atoms /cm², at an energy between 1 keV and 10 keV.
23
24 18. (PREVIOUSLY PRESENTED) The method of claim 1 wherein the doped
25 depletion region implantation is performed by implanting As or P ions at a
26 dose between 5E12 and 5E13 atoms/cm², at an energy between 100 keV

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- 1 and 500 keV; said doped depletion region having a minimum depth below
2 a surface of said substrate between 0.09 and 0.7 μm .
- 3
- 4 19. (PREVIOUSLY PRESENTED) The method of claim 1 wherein the doped
5 depletion region implantation is performed by implanting boron ions at a
6 dose between 5E11 and 5E13 atoms/cm², at an energy between 50 keV
7 and 200 keV; said doped depletion region having a minimum depth below a
8 surface of the substrate between 0.09 and 0.7 μm .
- 9
- 10 20. (PREVIOUSLY PRESENTED) The method of claim 1 wherein the S/D
11 implantation is performed by implanting arsenic (As) or phosphorus (P) ions
12 at a dose between 5E14 to 1E16 atoms/cm², at an energy between 50 keV
13 and 80 keV; said source and drain regions having a depth below a surface
14 of said substrate of between 0.04 and 0.5 μm .
- 15
- 16 21. (CURRENTLY AMENDED) The method of claim 1 wherein said second
17 conductivity type is p-type; and said S/D implant implantation is performed
18 by implanting boron ions at a dose between 5E14 to 1E16 atoms/cm², at an
19 energy between 50keV and 80keV; said source and drain regions have a
20 depth below a surface of said substrate of between 0.04 and 0.5 μm .
- 21
- 22 22. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
23 said gate structure having sidewalls; and forming one or more spacers on
24 the sidewalls of said gate structure.

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- 1
2 23. (CURRENTLY AMENDED) A method of forming a semiconductor device
3 comprising:
4 a) forming a gate structure over a substrate being doped with a first
5 conductivity type impurity;
6 b) performing a doped depletion region implantation by implanting ions being
7 a second conductivity type to the substrate to form doped depletion
8 regions beneath and separated from said source[/] and drain regions;
9 (1) said doped depletion regions have an impurity concentration and
10 thickness so that said doped depletion regions are depleted due to
11 a built-in potential created between said doped depletion regions
12 and said substrate; and
13 c) performing a S/D implantation by implanting ions being the second
14 conductivity type into the substrate to form said source and drain
15 regions adjacent to said gate structure;
16 (1) said substrate between said source and drain regions and said
17 doped depletion regions has a concentration of a first type impurity
18 between 1E16 to 1E18 atom/cc;
19 said doped depletion regions have an impurity concentration so that
20 the built-in potential between said doped depletion regions and said
21 substrate forms depletion regions in the substrate between the
22 source and drain regions and the doped depletion region regions;
23 said depletion regions have a net impurity concentration of the first
24 conductivity type; said depletion regions have a net impurity
25 concentration between 1E16 to 1E18 atom/cc.
26
27 24. (PREVIOUSLY PRESENTED) The method of claim 23 wherein said doped
28 depletion regions are not formed under said gate structure.
29

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- 1 25. (CURRENTLY AMENDED) The method of claim 23 wherein a region of said
2 substrate between said source[/] and drain regions and said doped
3 depletion regions has a concentration of said first conductivity type
4 impurity between 1E16 to 1E18 atom/cc;
5 a channel region in said substrate under said gate structure; said channel
6 region has a concentration of a second conductivity type impurity between
7 1E16 to 1E18 atom/cc.
- 8
- 9 26. (PREVIOUSLY PRESENTED) The method of claim 23 which further
10 includes; said gate structure has sidewalls; forming one or more spacers
11 on the sidewalls of said gate structure.
- 12
- 13 27. (PREVIOUSLY PRESENTED) The method of claim 23 which further
14 includes; said gate structure has sidewalls; forming two or more spacers
15 on the sidewalls of said gate structure prior to the doped depletion region
16 implantation.
- 17
- 18 **CLAIMS 28 TO 35 (CANCELED)**
- 19
- 20 **CLAIM 36 (CANCELED)**
- 21
- 22 37. (PREVIOUSLY PRESENTED) The method of claim 1 which further includes
23 said gate structure has sidewalls; forming two or more spacers on the
24 sidewalls of said gate structure prior to the doped depletion region
25 implantation.
- 26
- 27 38. (CURRENTLY AMENDED) A method of forming a semiconductor device
28 comprising:
29 forming a gate structure over a substrate being doped with a first
30 conductivity type impurity;

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- 1 performing a doped depletion region implantation by, using said gate
2 structure as an implant mask and implanting ions being of a second
3 conductive type into the substrate to form doped depletion regions;
4 and
5 performing a S/D implantation by implanting ions of the second
6 conductivity type into the substrate to form source and drain
7 regions adjacent to said gate;
8 the doped depletion regions are beneath and separated from said source
9 and drain regions; said doped depletion regions have an impurity
10 concentration and thickness so that said doped depletion regions
11 are depleted due to a built-in potential created between said doped
12 depletion regions and said substrate.
13
14 39. (PREVIOUSLY PRESENTED) The method of claim 38 which further
15 includes said doped depletion regions having an impurity concentration so
16 that a built-in junction potential between said doped depletion regions and
17 said substrate forms depletion regions in the substrate between the
18 source and drain regions and the doped depletion regions;
19 said depletion regions have a net impurity concentration of the first
20 conductivity type.
21
22 40. (PREVIOUSLY PRESENTED) The method of claim 38 wherein said doped
23 depletion regions are fully depleted.
24
25 41. (NEW) The method of claim 1, further comprising a channel region in said
26 substrate under said gate structure; wherein said heavily doped depletion
27 regions are not directly beneath said channel region.
28

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- 1 42. (NEW) The method of claim 23, wherein at least a portion of the doped
2 depletion regions are directly beneath and separated from said source and
3 drain regions.
- 4
- 5 43. (NEW) A method of forming a semiconductor device comprising:
6 a) forming a gate structure over a substrate being doped with a first
7 conductivity type impurity;
8 b) performing a doped depletion region implantation by implanting ions being
9 a second conductive type into the substrate to form doped depletion
10 regions;
11 c) performing a S/D implantation by implanting ions being the second
12 conductivity type into the substrate to form source and drain regions
13 adjacent to said gate structure; the doped depletion regions are
14 beneath and separated from said source and drain regions; and
15 d) performing LDD implantation by implanting ions being the second
16 conductive type into the substrate using the gate structure as a mask to
17 form LDD regions;
18 (1) said doped depletion regions having an impurity concentration and
19 thickness so that said doped depletion regions are depleted due to a
20 built-in potential created between said doped depletion regions and
21 said substrate;
22 said doped depletion regions having an impurity concentration so that a
23 built-in junction potential between said doped depletion regions and
24 said substrate forms depletion regions in the substrate between the
25 source and drain regions and the doped depletion regions;
26 said depletion regions have a net impurity concentration of the first
27 conductivity type.
- 28
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